The Impact Of Signal Jumping From A Reference Ground Plane To A Different Reference Ground Plane On Signal Integrity With A High-Impedance Load

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Abstract—**Oftentimes, it is necessary to route a signal between a ground plane and a second, different, ground plane. In such cases, an impedance discontinuity exists at the location where the signal jumps between the two reference planes. This discontinuity causes reflections between the source and this discontinuity, as well as between the load and this discontinuity. These reflections do not exist, however, when both the source and the load are matched to their transmission line segments. This paper discusses the signal integrity degradations that will occur when the source is matched to its transmission line segment, however, the load is not matched to its transmission line segment, and presents a high impedance load to this line. The model that is used throughout the analyses presented in this paper is a physics-based model that enables a physical understanding of the degradations.**

I. Introduction

When routing a signal throughout a printed circuit board, it is very possible that this signal may need to be routed between a ground plane and a second, different, ground plane. In this situation, an impedance discontinuity exists at the location of this kind of signal jumping. As a result of this impedance discontinuity, reflections will occur between this discontinuity and either the source or the load. If both the source and the load are matched to their transmission line segments, then no reflections will occur at either the source or load locations. This paper discusses the signal integrity degradations that can occur when the source is matched to its transmission line segment, however, the load presents a high-impedance load to its transmission line segment. In this case, reflections will exist at the load. Figure 1 highlights the physics-based model that is used to generate the computer simulations that are shown in this paper.

Figure 1 shows the situation in which the signal conductor is closest to the first ground plane for part of the transmission path, and is then closest to a second, different, ground plane for the remainder of the path. In this case, it becomes necessary to understand how the return current follows the outgoing signal current in order to determine any degradations of the signal integrity of the input signal as it propagates to the output load. Figure 1 depicts this situation in which the outgoing signal current jumps from signal layer 1 to signal layer 2 through the use of an electrical via.

Due to two different reference planes being used on the return path, an impedance discontinuity arises at the location of the electrical via that enables this kind of signal jumping. This impedance discontinuity is due to the signal via between the two ground planes, as well as the ground via that interconnects the two ground planes. Near the signal via, the ground via enables the return current to follow alongside the signal via.

In addition to the ground via, parasitic capacitances (C_{via}) also occur between the signal via and the two reference planes. Together, these impedances can be incorporated into an equivalent circuit model as shown in Figure 1. In this model, the impedance discontinuity between the two reference planes is modeled as a parasitic inductance ($L_{p\text{-}g}$). Similarly, the via between the two signal layers is also modeled as an inductance (L_{via}). It is well known in the industry that the barrel of vias can be modeled as inductors from an impedance perspective.

II. Simulation Results

It is of interest to understand the signal degradations imposed on the received output signal when the load of the transmission line is a high-impedance load, and in which only the first reflection from the load to the signal via and then back to the load is considered. The parameters specifying the above transmission line discontinuity are entered directly into a Mathcad worksheet that performs the computer simulations. All of the plots throughout this paper were generated from a Mathcad worksheet that was written by the author and is available at the following website: www.the-signal-and-power-integrity-institute.com. Figure 2 shows the simulation results where C_{via}=0.1pF, L_{via}=1.0nH, $L_{p\text{-}g}$=1nH. In addition, the bit rate is 1Gbs, the risetime of the propagating signal at the output of the source is 150ps, and the length of the transmission line is 5inches. The high impedance load is

2.5inches from the discontinuity. Figure 3 shows the associated eye pattern s.

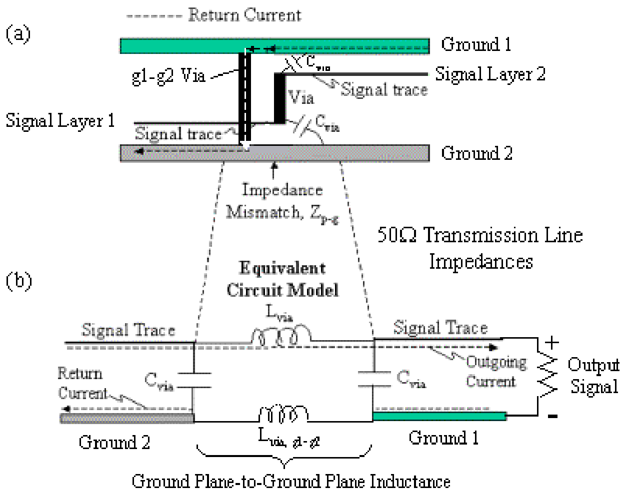

Figure 1

Fig. 1. A physics-based model that characterizes signal jumping between a ground plane and a power plane.

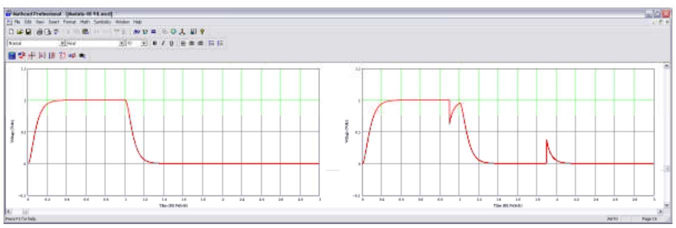

Fig. 2. Load waveform (right), and source waveform (left) at 1Gbs, and with C_{via}=0.1pF, L_{via}=1.0nH, L_{p-g}=1nH. The risetime of the source signal is 150ps.

Figure 4 shows the results from the case in which only C_{via} is decreased from 0.1pF to 0.07pF. Figure 5 shows the associated eye patterns. As can be seen from Figure 4, decreasing the parasitic via capacitances causes better signal integrity performances. A value of 0.1pF for C_{via} can be realized with a via diameter of 5mils, a via pad diameter of 15mils, and an antipad diameter of about 28mils. These values are very reasonable. Increasing the antipad diameter to 50mils decreases C_{via} to about 0.07pF.

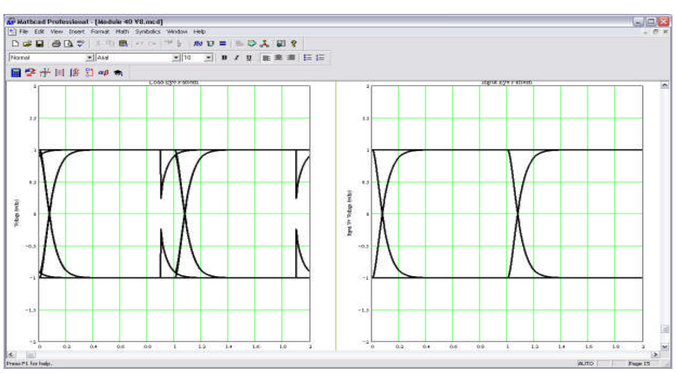

Fig. 3. Load eye pattern (le ft), and source eye pattern (right) at 1Gbs, and with C_{via}=0.1pF, L_{via}=1.0nH, and L_{p-g}=1nH.

Since the load is far from the discontinuity, the signal degradations occur along the falltime. If the load is placed 0.25inches from the discontinuity, then Figure 6 shows the results. In this case the timing jitter is greatly increased due to the location of the load relative to the signal via.

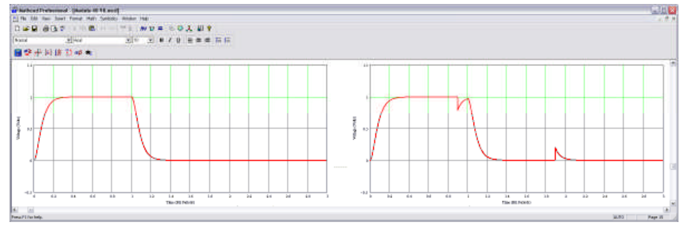

Fig. 4. Load waveform (right), and source waveform (left) at 1Gbs, and with C_{via}=0.07pF, L_{via}=1.0nH, L_{p-g}=1nH. The risetime of the source signal is 150ps.

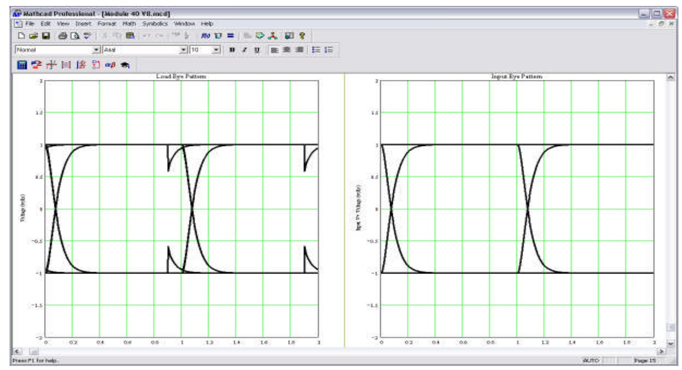

Fig. 5. Load eye pattern (left), and source eye pattern (right) at 1Gbs, and with C_{via}=0.0 7pF, L_{via}=1.0nH, and L_{p-g}=1nH.

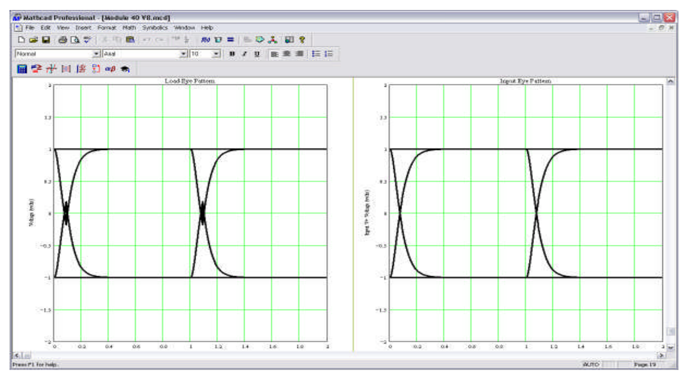

Fig. 6. Load eye pattern (left), and source eye pattern (right) at 1Gbs, and with C_{via}=0.07pF, L_{via}=1.0nH, and L_{p-g}=1nH. The load is 0.25inches from the signal via.

Figure 7 shows the eye patterns for the case in which only the bit rate has been increased from 1Gbs to 2Gbs. Finally, Figure 8 highlights the results in which only the distance from the load to the signal via has been increased from 0.25inches to 1.0inch. In this situation, the degradation occurs near the middle of the eye pattern, and does not increase the timing jitter. Figure 9 shows the results when the distance between the signal via and the load is increased to 1.275inches. In this case, the eye pattern for the load is optimal in the sense that the degradation did not increase the timing jitter, nor should it affect the bit-error-rate performance of the system if the eye pattern for the load is sampled near the middle of its eye opening when making bit decisions.

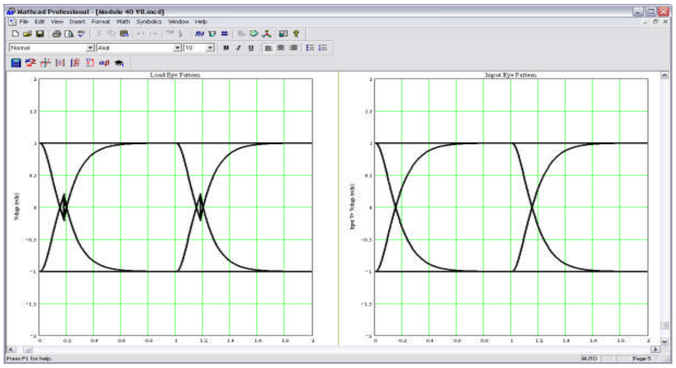

Fig. 7. Load eye pattern (left), and source eye pattern (right) at 2Gbs, and with C_{via}=0.7pF, L_{via}=1.0nH, and $L_{p\text{-}g}$=1nH. The load is 0.25inches from the signal via.

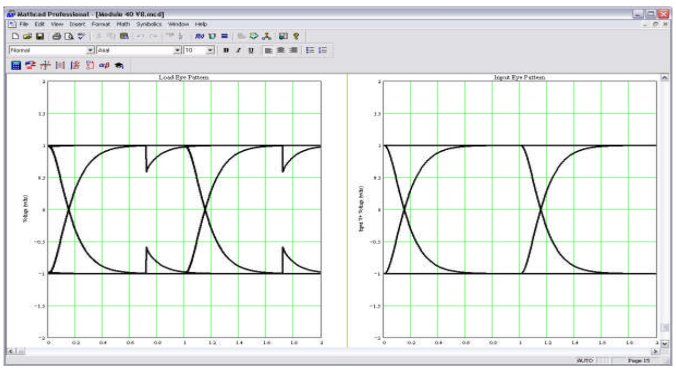

Fig. 8. Load eye pattern (left), and source eye pattern (right) at 2Gbs, and with C_{via}=0.07pF, L_{via}=1.0nH, and $L_{p\text{-}g}$=1nH. The load is 1.0inches from the signal via.

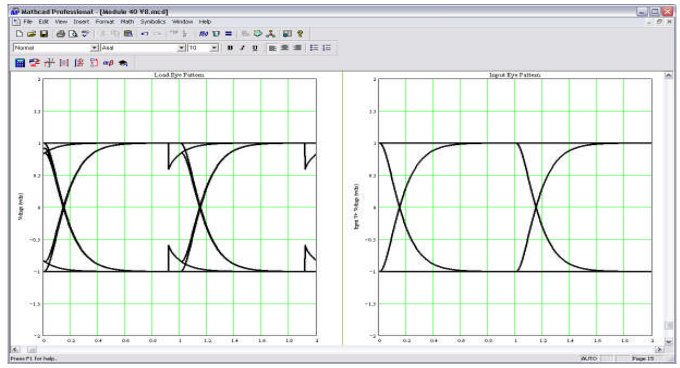

Fig. 9. Load eye pattern (left), and source eye pattern (right) at 2Gbs, and with C_{via}=0.07pF, L_{via}=1.0nH, and $L_{p\text{-}g}$=1nH. The load is 1.275inches from the signal via.

III. Conclusions

Based upon the previous research, it was disclosed that signal jumping between two different ground planes with a high impedance load can cause significant signal degradations on the received output signal if the load is not properly displaced from the signal via. Depending upon the location of the load relative to the discontinuity, the degradations could occur along the risetime or other part of the signal. It was then shown that the signal degradations increase with increasing bit rates, as well as increasing via parasitic capacitances. As long as the degradations occur such that they don't increase the timing jitter, nor reduce the maximum eye opening near the middle of the eye pattern, then these degradations can be mostly tolerated. The material covered throughout this paper can be studied through the interactive signal integrity learning environment that is available at www.the-signal-and-power-integrity-institute.com .