The Impact Of Signal Jumping From A Reference Ground Plane To A Reference Power Plane On Signal Integrity With A High-Impedance Load

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***Abstract*—Oftentimes, it is necessary to route a signal between a power plane and a ground plane. In such cases, an impedance discontinuity exists at the location where the signal jumps between the two reference planes. This discontinuity causes reflections between the source and this discontinuity, as well as between the load and this discontinuity. These reflections do not exist, however, when both the source and the load are matched to their transmission line segments. This paper discusses the signal integrity degradations that will occur when the source is matched to its transmission line segment, however, the load is not matched to its transmission line segment, and presents a high impedance load to this line. The model that is used throughout the analyses presented in this paper is a physics-based model that enables a physical understanding of the degradations.**

I. Introduction

When routing a signal throughout a printed circuit board, it is very possible that this signal may need to be routed between a ground plane and a power plane. In this situation, an impedance discontinuity exists at the location of this kind of signal jumping. As a result of this impedance discontinuity, reflections will occur between this discontinuity and either the source or the load. If both the source and the load are matched to their transmission line segments, then no reflections will occur at either the source or load locations. This paper discusses the signal integrity degradations that can occur when the source is matched to its transmission line segment, however, the load presents a high-impedance load to its transmission line segment. In this case, reflections will exist at the load. Figure 1 highlights the physics-based model that is used to generate the computer simulations that are shown in this paper.

Figure 1 shows the situation in which the signal conductor is closest to the power plane for part of the transmission path, and is then closest to the ground plane for the remainder of the path. In this case, it becomes necessary to understand how the return current follows the outgoing signal current in order to determine any degradations of the signal integrity of the input signal as it propagates to the output load. Figure 1 depicts this situation in which the outgoing signal current jumps from signal layer 1 to signal layer 2 through the use of an electrical via.

Due to two different reference planes being used on the return path, an impedance discontinuity arises at the location of the electrical via. This impedance discontinuity is due to the capacitance between the power and ground planes. Near the via, a displacement current component will allow the return current to follow alongside the via until it encounters the power plane, in which the power plane then carries the return current alongside the outgoing signal current. This displacement current is due to an external surface mountable capacitor that is near to the signal via.

In addition to the local capacitance between the power and ground planes, parasitic capacitances (C_{via}) also occur between the signal via and the two reference planes. Together, these impedances can be incorporated into an equivalent circuit model as shown in Figure 1. In this model, the impedance discontinuity between the two reference planes is modeled as a parasitic inductance between the power and ground planes (L_{p-g}), in series with a parasitic resistive component (R_{p-g}), and the surface mountable capacitance (C_{p-g}). Similarly, the via between the two signal layers is also modeled as an inductance (L_{via}). It is well known in the industry that the barrel of vias can be modeled as inductors from an impedance perspective.

II. Simulation Results

It is of interest to understand the signal degradations imposed on the received output signal when the load of the transmission line is a high-impedance load, and in which only the first reflection from the load to the via and then back to the load is considered. The parameters specifying the above transmission line discontinuity are entered directly into a Mathcad worksheet that performs the computer simulations. All of the plots throughout this paper were generated from a Mathcad worksheet that was written by the author and is available at the following website: www.the-signal-and-power-integrity-institute.com. Figure 2 shows the simulation results where C_{via}=0.5pF, L_{via}=1.0nH, L_{p-g}=1nH, C_{p-g}=0.1μF, and R_{p-g}=0.2Ω. In addition, the bit rate is 200Mbs, the risetime of the propagating signal at the output of the source is

100ps, and the length of the transmission line is 5inches. The high impedance load is 0.5inches from the discontinuity.

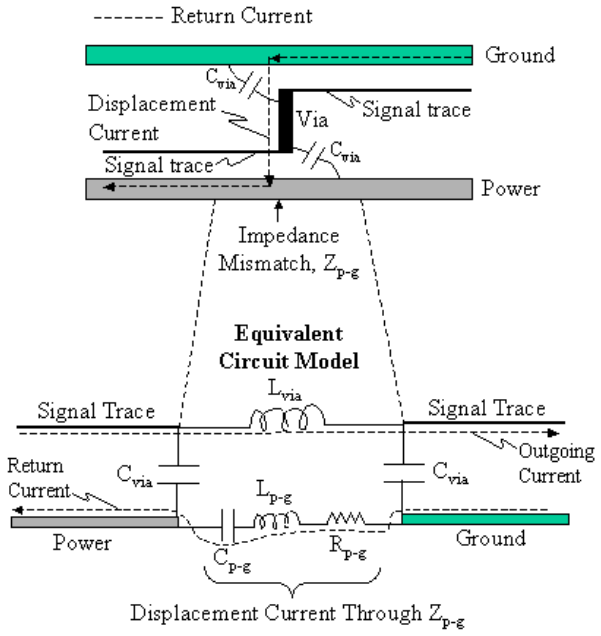

Fig. 1. A physics-based model that characterizes signal jumping between a ground plane and a power plane.

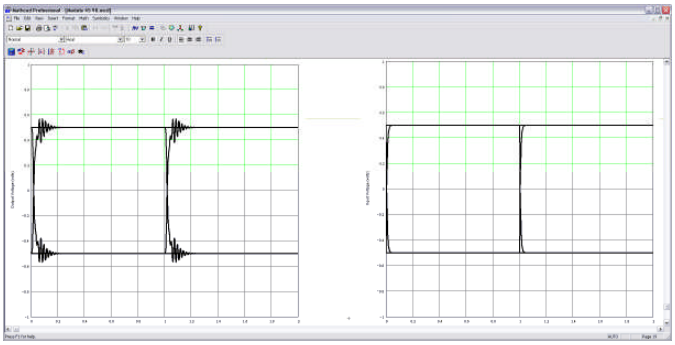

Fig. 2. Load eye pattern (left), and source eye pattern (right) at 200Mbs, and with C_{via}=0.5pF, L_{via}=1.0nH, L_{p-g}=1nH, C_{p-g}=0.1μF, and R_{p-g}=0.2Ω. The risetime of the source signal is 100ps.

Figure 3 shows the results from the case in which only C_{via} is increased from 0.5pF to 1.0pF. As can be seen from Fig. 3, increased parasitic via capacitances causes more signal ringing.

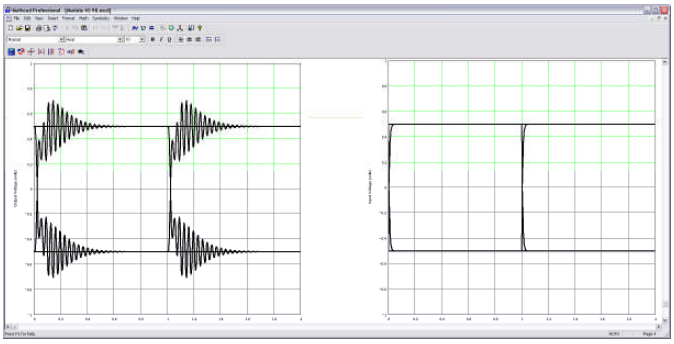

Fig. 3. Load eye pattern (left), and source eye pattern (right) at 200Mbs, and with C_{via}=1.0pF, L_{via}=1.0nH, L_{p-g}=1nH, C_{p-g}=0.1μF, and R_{p-g}=0.2Ω. The risetime of the source signal is 100ps.

Since the load is very close to the discontinuity, the ringing occurs partly along the risetime. If the load is placed 2.5inches from the discontinuity, then Fig. 4 shows the results. If the bit rate is increased to 1Gbs, then Fig. 5 highlights the performance of this system. Figure 6 shows the results when the bit rate is 2Gbs. If the parasitic via capacitance is reduced from 1pF to 0.5pF, then Figure 7 highlights the performance.

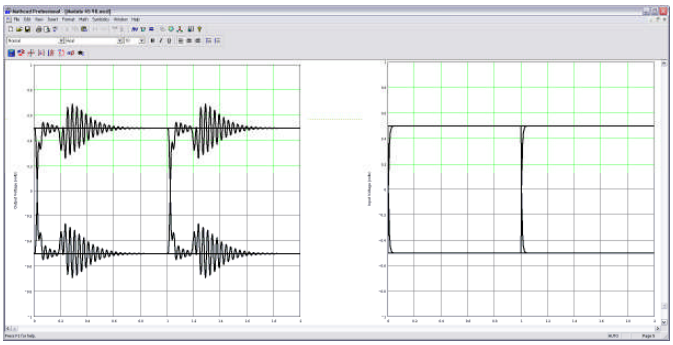

Fig. 4. Load eye pattern (left), and source eye pattern (right) at 200Mbs, and with C_{via}=1.0pF, L_{via}=1.0nH, L_{p-g}=1nH, C_{p-g}=0.1μF, and R_{p-g}=0.2Ω. The risetime of the source signal is 100ps.

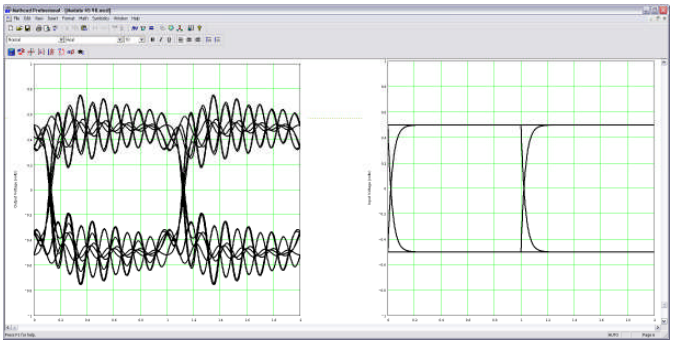

Fig. 5. Load eye pattern (left), and source eye pattern (right) at 1Gbs, and with C_{via}=1.0pF, L_{via}=1.0nH, L_{p-g}=1nH, C_{p-g}=0.1μF, and R_{p-g}=0.2Ω. The risetime of the source signal is 100ps.

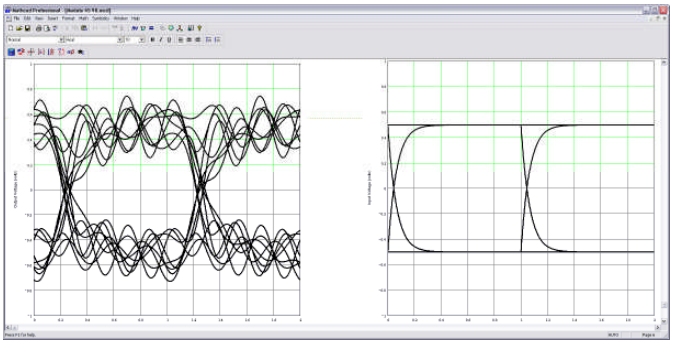

Fig. 6. Load eye pattern (left), and source eye pattern (right) at 2Gbs, and with C_{via}=1.0pF, L_{via}=1.0nH, L_{p-g}=1nH, C_{p-g}=0.1μF, and R_{p-g}=0.2Ω. The risetime of the source signal is 100ps.

Figure 8 highlights the results when C_{via} is decreased further to 0.1pF. In this case, the output eye pattern is significantly improved, with a noticeable reduction in the timing jitter.

However, undershoot and overshoot are also present in the eye pattern.

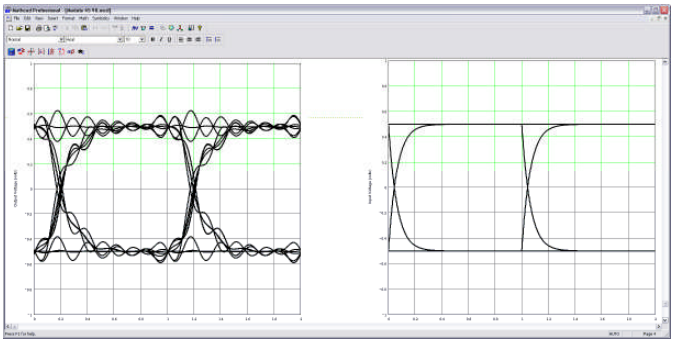

Fig. 7. Load eye pattern (left), and source eye pattern (right) at 2Gbs, and with C_{via}=0.5pF, L_{via}=1.0nH, L_{p-g}=1nH, C_{p-g}=0.1μF, and R_{p-g}=0.2Ω. The risetime of the source signal is 100ps.

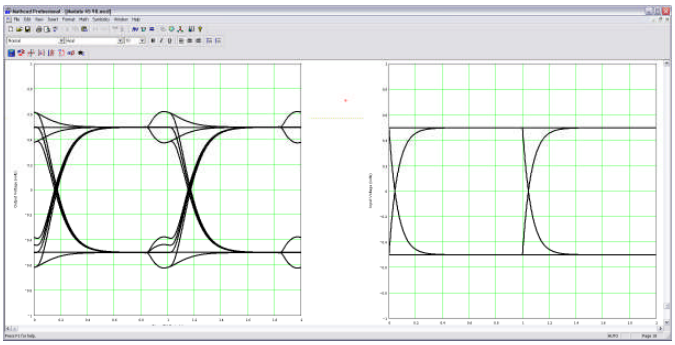

Fig. 8. Load eye pattern (left), and source eye pattern (right) at 2Gbs, and with C_{via}=0.1pF, L_{via}=1.0nH, L_{p-g}=1nH, C_{p-g}=0.1μF, and R_{p-g}=0.2Ω. The risetime of the source signal is 100ps.

If C_{p-g} is reduced from 0.1μF to 100pF, while decreasing its mounting inductance from 1nH to 0.2nH, then Figure 9 highlights the performance. This kind of capacitance and mounting inductance can be obtained with 0201 capacitors. Note that the timing jitter has been further reduced, as well as the overshoot and undershoot. The noise margin has been slightly reduced in magnitude.

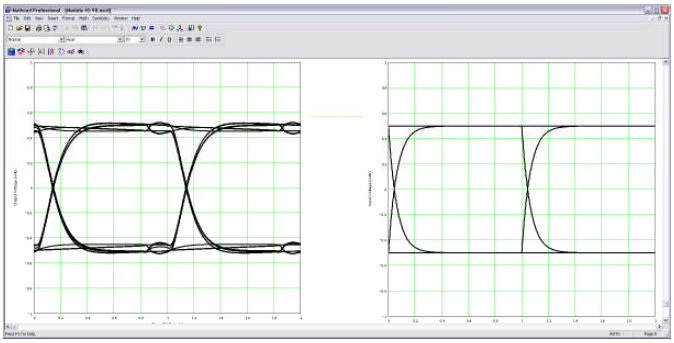

Fig. 9. Load eye pattern (left), and source eye pattern (right) at 2Gbs, and with C_{via}=0.1pF, L_{via}=1.0nH, L_{p-g}=0.2nH, C_{p-g}=100pF, and R_{p-g}=0.2Ω. The risetime of the source signal is 100ps.

III. Conclusions

Based upon the previous research, it was disclosed that signal jumping between a ground plane and a power plane with a high impedance load can cause significant signal degradations on the received output signal. Depending upon the location of the load relative to the discontinuity, the degradations could occur along the risetime or other part of the signal. It was then shown that the signal degradations increase with increasing bit rates, as well as increasing via parasitic capacitances. Finally, it was shown that small 0201 capacitors with 100pF of capacitance, as well as small mounting inductances of about 0.2nH can produce very good signal integrity performances. The material covered throughout this paper can be studied through the interactive signal integrity learning environment that is available at www.the-signal-and-power-integrity-institute.com .