Low Impedance Clock Distribution Networks

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***Abstract*—In many data applications, it is necessary to distribute a clock signal to several different loads. One approach to performing such a task is to create a low impedance serial bus that carries the clock signal, and then form taps off of this bus to send the various clock signals to the various loads. This paper discusses the signal integrity performance of such a clock distribution system when a 100MHz clock signal, with a 1ns risetime, is tapped three times along a 6inch long clock serial bus. The three distribution loads are high impedance loads, and their tap lengths, and load characteristics are varied to reflect the design situation under consideration.**

I. Introduction

This paper treats the application of distributing a clock signal to three identical receivers, in which each receiver is modeled as having an input impedance equal to a series R-L-C circuit. This configuration is shown in Figure 1. The R-L-C circuit provides the most flexibility in modeling the input impedances of the receivers plus the parasitic elements associated with the tap or interconnect. For example, the C component can model the capacitance due to tapping the main line plus the receiver input capacitance. In addition, the R and L components can model the parasitic resistive and inductive components from the tap plus the resistive and inductive components of the receiver's input impedance. Oftentimes, this kind of clock distribution network requires the impedance of the main line to be less than 50ohms. Therefore, this clock distribution network is referred to as a low impedance distribution network. Of course, more receivers could have been added to this network, however, with only three receivers, general transmission principles can be extracted that apply to more than three receivers.

This paper addresses the various elements that contribute to the signal integrity of the received clock signals. For example, the input risetimes, propagation delays (Td), the R-L-C values, as well as the transmission line bandwidth and driver and load impedances can all be adjusted to learn about the signal integrity properties of this clock distribution network. The signal integrity information is displayed in both the frequency and time domains. The magnitude of the S_{21} transfer functions, as well as the phase responses for each receiver are shown in order to extract signal attenuation, propagation delay, and possible pulse dispersion information for each receiver. The time domain information for each receiver is shown in the form of the received clock waveforms over one clock cycle.

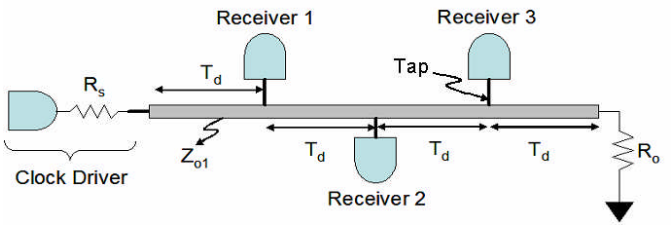

Fig. 1. Low impedance clock distribution network with three receivers.

II. Simulation Results

The first situation considered is when the propagating clock signal is characterized with a 100MHz frequency, a 1ns risetime, and the length of the bus is 6inches. Each receiver is characterized with an input impedance, including the interconnect impedance, that is modelled by a series R-L-C circuit in which R=14mΩ, L=2nH, and C=0.7pF. The bus impedance is 20Ω. In addition, R_o=20Ω, and the clock driver output impedance is also 20Ω. Since both the far end of the clock bus, as well as the clock driver, are both matched to the bus impedance, we are focusing on the signal integrity degradations due solely to the other design parameters. The 6inch bus length is divided into four 1.5inch segments, in which the three receivers are placed at 1.5inches, 3.0inches, and then 4.5inches from the source. In addition, the length of the tap from the bus to each receiver is 0.1inches. For this situation, Figure 2 highlights the received clock waveforms for the first two receivers. The third receiver's clock signal is identical to the first receiver's clock waveform.

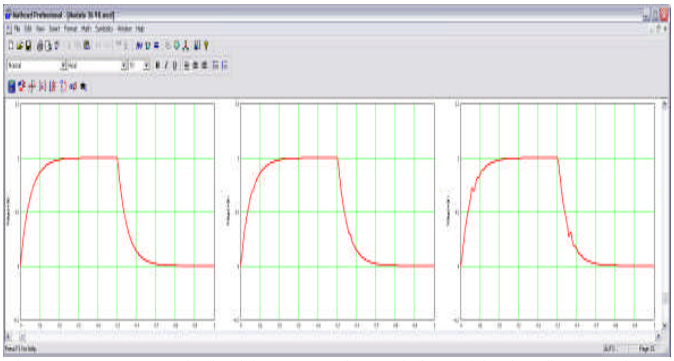

Fig. 2. 100MHz clock driver waveform (left), with the first receiver's waveform (middle), and the second receiver's waveform (right). The bus impedance is 20Ω.

As can be seen from Figure 2, only the clock signal from the second receiver shows any signal degradations, and they occur along the rising and falling edges. However, these degradations are negligible. Figure 3 shows the received clock signals when the bus impedance is increased from 20Ω to 30Ω. Figure 4 shows the received clock signals when the bus impedance is increased from 30Ω to 40Ω. Figure 5 shows the received clock signals when the bus impedance is increased further from 40Ω to 50Ω.

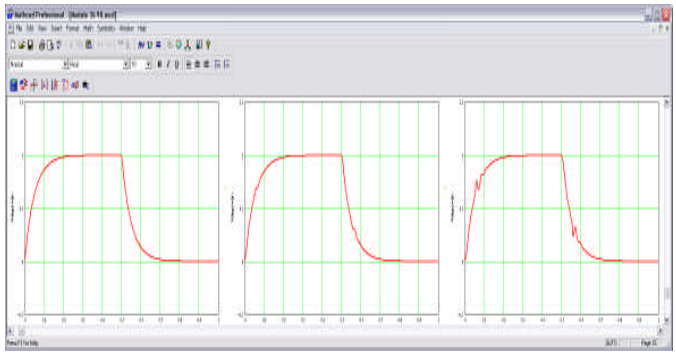

Fig. 3. 100MHz clock driver waveform (left), with the first receiver's waveform (middle), and the second receiver's waveform (right). The bus impedance is 30Ω.

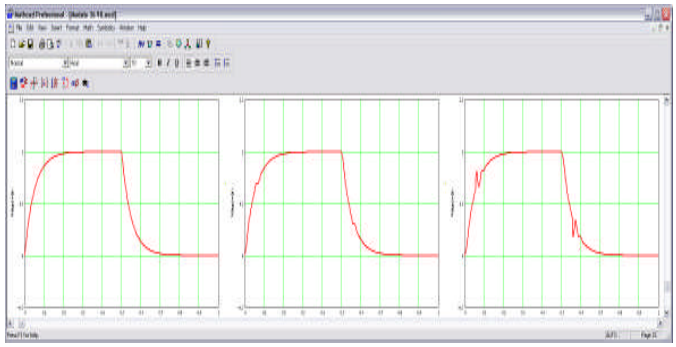

Fig. 4. 100MHz clock driver waveform (left), with the first receiver's waveform (middle), and the second receiver's waveform (right). The bus impedance is 40Ω.

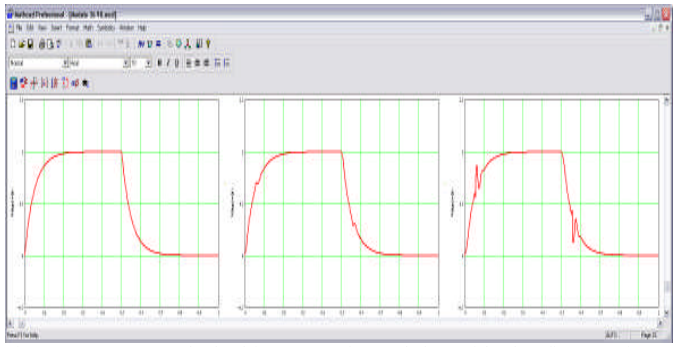

Fig. 5. 100MHz clock driver waveform (left), with the first receiver's waveform (middle), and the second receiver's waveform (right). The bus impedance is 50Ω.

As can be seen from Figures 2-5, increasing the bus impedance caused increased signal degradations, especially on the second receiver's signal. The first receiver's signal, however, is very robust against changes in the bus impedance.

Next, reconsider the values of the system variables that led to the results shown in Figure 2. Figure 6 shows the results when only the lengths of each tap are increased from 0.1inches to 0.3inches.

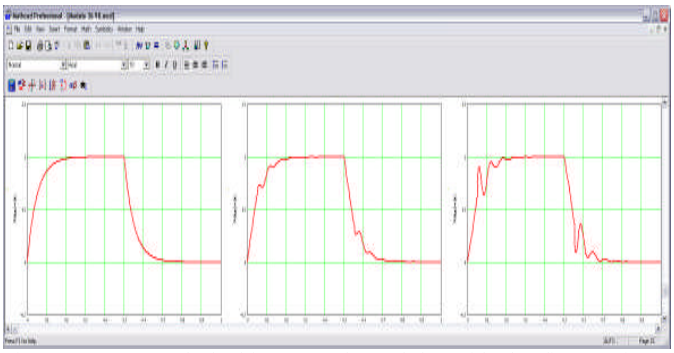

Fig. 6. 100MHz clock driver waveform (left), with the first receiver's waveform (middle), and the second receiver's waveform (right). The bus impedance is 20Ω, and the lengths of the three taps have been increased from 0.1inches to 0.3inches.

Figure 6 clearly highlights the sensitivity of the received clock signals on the length of the taps. In this case, a tap length of only 0.3inches caused significant signal degradations on the second receiver's waveform. Figure 7 shows the results when the tap length if further increased to 0.5inches.

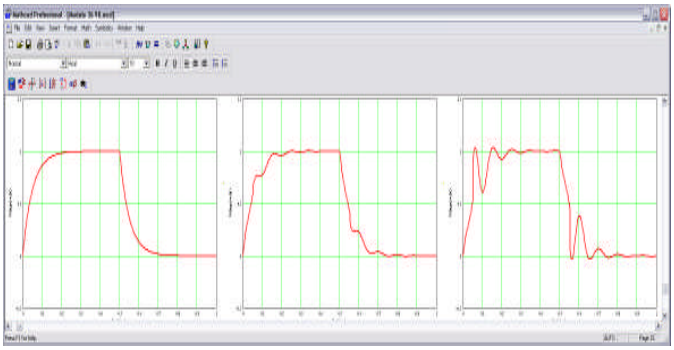

Fig. 7. 100MHz clock driver waveform (left), with the first receiver's waveform (middle), and the second receiver's waveform (right). The bus impedance is 20Ω, and the lengths of the three taps have been increased from 0.3inches to 0.5inches.

According to Figure 7, the clock signal for the second receiver is significantly degraded, and may not be able to drive its load. Therefore, it appears that in order for this clock distribution system to work well, the bus impedance should be low, and the tap lengths should be less than about 0.2 inches. If the clock frequency is reduced from 100MHz to 20MHz, then Figure 8 highlights the received clock waveforms when the tap lengths are 0.5inches. It appears that lowering the clock frequency does not improve the performance of this low impedance clock distribution system when the tap lengths are 0.5inches long.

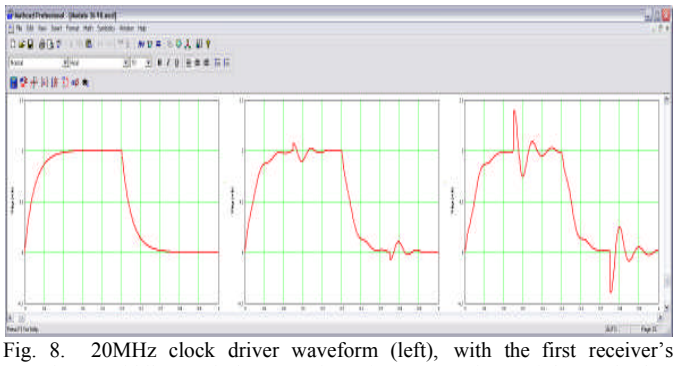

Fig. 8. 20MHz clock driver waveform (left), with the first receiver's waveform (middle), and the second receiver's waveform (right). The bus impedance is 20Ω, and the lengths of the three taps are all equal to 0.5inches.

III. CONCLUSIONS

Based upon the previous research, it was disclosed that low impedance serial bus clock distribution systems work well whenever the bus impedance is less than about 30Ω, and when the tap lengths are no more than about 0.2inches. These conclusions were observed for clock frequencies up to 100MHz. Receivers that are located between the first and last receivers experience the worst signal degradations. The material presented in this paper can be studied through the interactive signal integrity learning environment that is available at the following website: www.the-signal-and-power-integrity-institute.com.