The Impact Of Asymmetrical TTL and CMOS Drivers On Signal Integrity For High Impedance Loads

David Norte, PhD

signalpowerintegrity@yahoo.com

***Abstract*—In many data applications, asymmetrical CMOS or TTL drivers are used to represent the data. In these cases, the output driver impedances are different in the High and Low states, and usually no attempt is made to match the driver to the transmission line. As such, it is of interest to understand the signal integrity performances of using these kinds of drivers with no transmission line matching. This paper highlights computer simulations that show the signal integrity considerations that should be taken into account when using such drivers.**

I. Introduction

In this paper, we study the impact of asymmetric CMOS and TTL driver output impedances on the signal integrity of the received signal when the load appears as a high impedance load, such as a very small capacitive load. The driver is assumed to be a CMOS or TTL driver in which the HIGH and LOW output impedances are different. The electrical interconnect between the driver and the load is characterized with an interconnect inductance and capacitance per unit length. The load capacitance is usually on the order of 0.01pF-2pF, creating a high-impedance load to the transmission line. In addition, the load series resistance is usually small, on the order of a few milliohms.

The driver output impedance can be determined from its IBIS model and is usually between 15ohms and about 165ohms, which corresponds to the low and high switching states of typical TTL and CMOS drivers. Depending upon the value of these impedances, it is possible to induce overshoot or undershoot on the received waveform. Since the driver output impedances for TTL and CMOS drivers vary dramatically between the HIGH and LOW signaling states, there is typically no attempt to terminate the driver with a series termination. Depending upon the one-way propagation delay, these signal degradations can either appear along the rising/falling edges of the received signal or along the lower-frequency portion of the received pulse.

In order to focus on the signal degradations due to the varying driver output impedances, and the high-impedance load, the bandwidth of the interconnect is also taken into account. This paper attempts to disclose the signal integrity degradations of typical TTL or CMOS drivers due to their widely varying output impedances. These output impedances can typically be determined from the datasheet for the driver. For example, if the V_{OL} and V_{OH} values are known, as well as the V_{CC} and the output drive current (I_{out}) for each state, then the "HIGH" and "LOW" output state impedances can be found from the following relationships for a CMOS inverter:

$$R_{HIGH} = (V_{CC} - V_{OH})/I_{out(High)}$$
$$R_{LOW} = V_{OL}/I_{out(Low)}$$

Once these values have been determined, then we can estimate the signal integrity degradations due to these two output impedances.

II. Simulation Results

The first situation considered is when the frequency of the propagating signal is 55MHz and the value of Vcc is 5V, whereas V_{OH} = 2.7V, V_{OL} = 0.4V, I_{OH} = 8ma, I_{OL} = 4ma, and the length of the 194Ω transmission line that carries the signal is 6inches. The risetime of the driver's signal is 1ns. The aforementioned voltage and current values are typical for the 74HC or 74HCT family of CMOS devices. In this case, R_{HIGH} = 287.5Ω and R_{LOW} = 100Ω. The transmission line impedance of 194Ω is the average of the HIGH and LOW driver impedances.

In this case, Figure 1 shows the load eye patterns for the asymmetrical CMOS driver (left), as well as a hypothetical CMOS driver in which R_{HIGH} = R_{LOW}, and the transmission line impedance is matched to this value (right). As can be seen from Figure 1, signal degradations occur along the rising and falling edges for the actual CMOS driver. It should also be mentioned that achieving this high transmission line impedance (194Ω) is nearly impossible, except for possibly thick printed circuit boards.

For instructional purposes, Figure 2 shows the eye patterns when the transmission line impedance is changed to 287.5Ω, which is equal to R_{HIGH}. In this case, the eye pattern for the load exhibits small overshoot, however, the signal quality along the risetime is significantly improved. It should again

be mentioned, however, that it is nearly impossible to achieve this large transmission line impedance in practice. On the other hand, Figure 3 shows the eye patterns when the transmission line impedance is set to 113Ω, which is close to R_{LOW}. This kind of impedance is not difficult to achieve in practice. For example, a microstripline with a distance to its reference plane equal to 17mils, and with a conductor width equal to 4mils will achieve an impedance close to 113Ω. In this case, the rising and falling edges exhibit excessive signal integrity degradations.

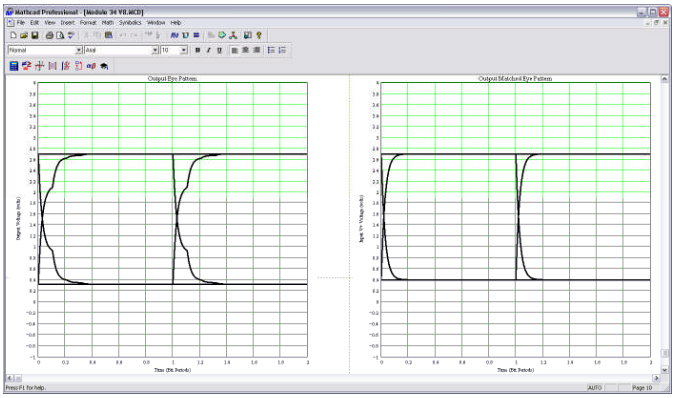

Fig. 1. 55Mbs load eye pattern for the asymmetrical CMOS driver (left), and the hypothetical symmetrical driver (right). The transmission line impedance is 194Ω, which is the average of R_{HIGH} and R_{LOW}.

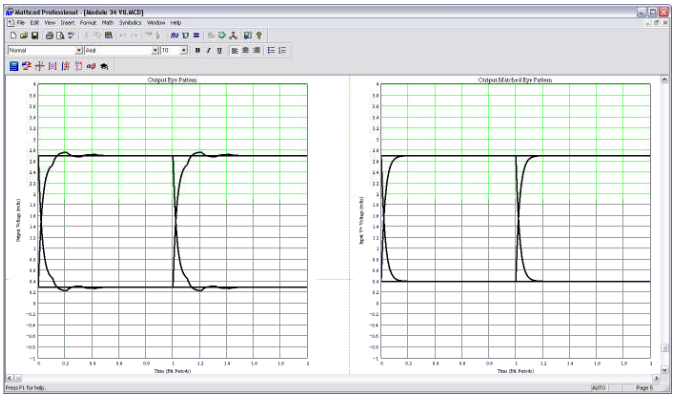

Fig. 2. 55Mbs load eye pattern for the asymmetrical CMOS driver (left), and the hypothetical symmetrical driver (right). The transmission line impedance is 287.5Ω, which is equal to R_{HIGH}.

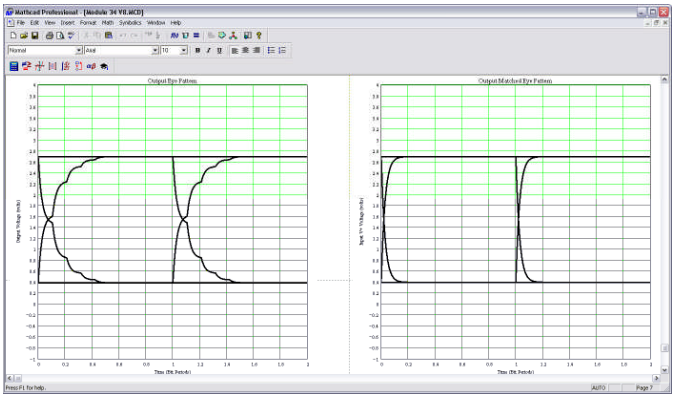

Fig. 3. 55Mbs load eye pattern for the asymmetrical CMOS driver (left), and the hypothetical symmetrical driver (right). The transmission line impedance is 113Ω, which is close to R_{LOW}.

At this point, it is clear that small risetimes of about 1ns or less lead to significant signal degradations along the rising and falling edges that may not be acceptable. Alternatively, Figure 4 shows the case in which the risetime of the 55Mbs data signal has been increased from 1ns to 5.5ns, and the transmission line impedance is still 113Ω. Figure 4 shows that larger risetimes cause much less signal degradations for the asymmetrical CMOS driver. Therefore, it appears that typical asymmetrical CMOS drivers require risetimes of at least about 5.5ns. Of course, if the gap between R_{HIGH} and R_{LOW} is made smaller, then it may be possible for the asymmetrical CMOS driver to support smaller risetimes.

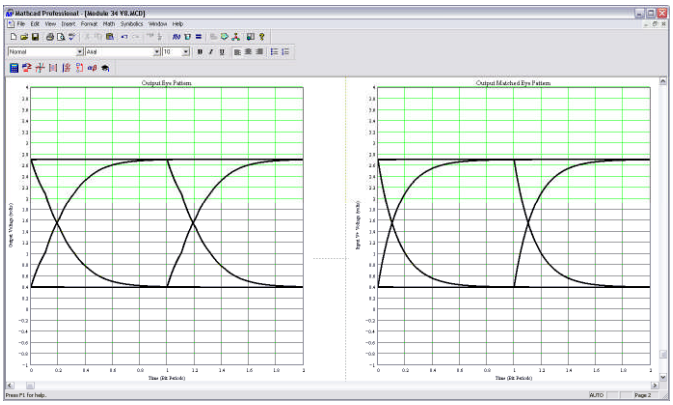

Fig. 4. 55Mbs load eye pattern for the actual CMOS driver (left), and the hypothetical driver (right). The transmission line impedance is 113Ω, which is close to R_{LOW}. R_{HIGH} is still equal to 287.5Ω.

For example, if R_{HIGH}=100Ω and R_{LOW}=175Ω, then Figure 5 shows the results when the transmission line impedance is still 113Ω, and the asymmetrical CMOS driver risetime has been decreased from 5.5ns to 3.5ns. As can be seen from Figure 5, the output eye pattern from the asymmetrical CMOS driver shows little signal degradations, and closely resembles the eye pattern from the hypothetical symmetrical CMOS driver.

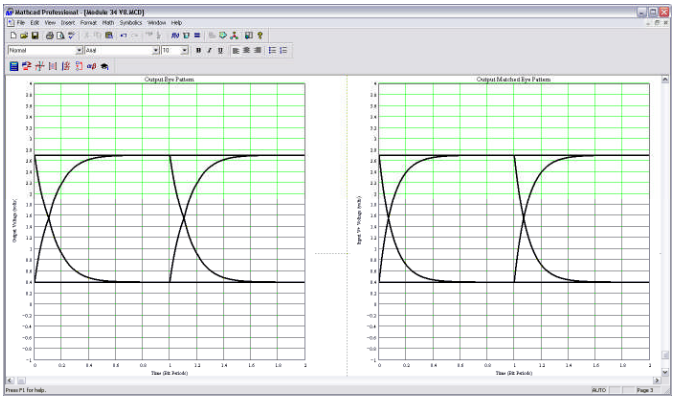

Fig. 5. 55Mbs load eye pattern for the actual CMOS driver (left), and the hypothetical driver (right). The transmission line impedance is 113Ω, which is close to R_{LOW}, and R_{HIGH} has been lowered to 175Ω, while the driver risetime has been reduced from 5.5ns to 3.5ns.

III. Conclusions

Based upon the previous research, it was disclosed that asymmetrical CMOS and TTL drivers, in which R_{HIGH} is not equal to R_{LOW}, can cause significant signal degradations when the driver risetime is less than about 1ns. Asymmetrical CMOS driver risetimes less than about 1ns can not be supported with practical transmission line impedances. On the other hand, it was shown that asymmetrical CMOS drivers, with practical transmission line impedances of about 113Ω, can produce excellent signal integrity performances as long as the driver risetime is at least about 5.5ns for typically encountered drivers. This result limits the operating frequency to about 50MHz. Of course, if fabrication technologies can close the gap between R_{HIGH} and R_{LOW}, then asymmetrical CMOS drivers might be used at higher frequencies. ECL drivers, for example, can be used at much higher frequencies because $R_{HIGH} = R_{LOW}$ for these kinds of drivers. The material presented in this paper can be studied through the interactive signal integrity learning environment that is available at the following website: www.the-signal-and-power-integrity-institute.com.