Determining The Impact Of Load Termination Resistor Location On Signal Integrity

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***Abstract*— It is of interest to understand the impact of the location of load termination resistors on the signal integrity of the received signal when the terminating resistor is placed away from the load. This paper discusses the signal integrity implications when the terminating resistor is placed before and away from the load, or near the load, or after and away from the load. This situation is commonly encountered when there is not enough printed circuit board area to place the terminating resistor close to the load, for example. Field programmable gate arrays are such an example in which the pin field is too dense to allow the placement of load termination resistors close to the loads. It is shown that when the termination resistor can not be placed close to the load, then it is better to place the resistor after and away from the load.**

I. INTRODUCTION

Figure 1 shows the situation in which a termination resistor is placed either before and away from the load, or after and away from the load. The placement of the termination resistor away from the load must be considered whenever the resistor can not be placed close to the load, such as within the pin field of an FPGA integrated circuit chip, for example.

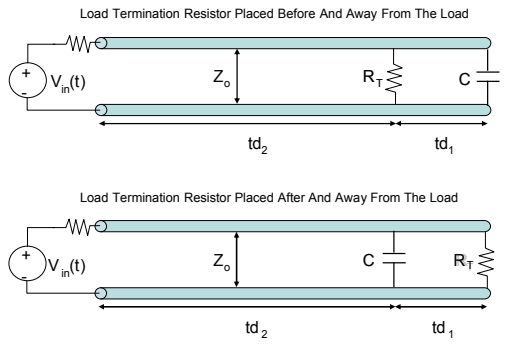

Figure 1

Figure 1 shows the time delays associated with this kind of design situation. In this case, the variable td_1 represents the time delay between the load and the termination resistor. It is of interest in this paper to determine the signal degradations that can occur under both situations.

II. SIMULATION RESULTS

The first situation considered is when the propagating signal is characterized with a 100Mbs bit rate and a 2ns risetime. The source resistance is 50Ω, and is matched to the 50Ω transmission line. The load is a high impedance load. The value of td_1 is 0.175ns, and the value of td_2 is 1.4ns. All of the plots throughout this paper were generated from a Mathcad worksheet that was written by the author and is available at the following website: www.the-signal-and-power-integrity-institute.com. Figure 2 shows the simulation results.

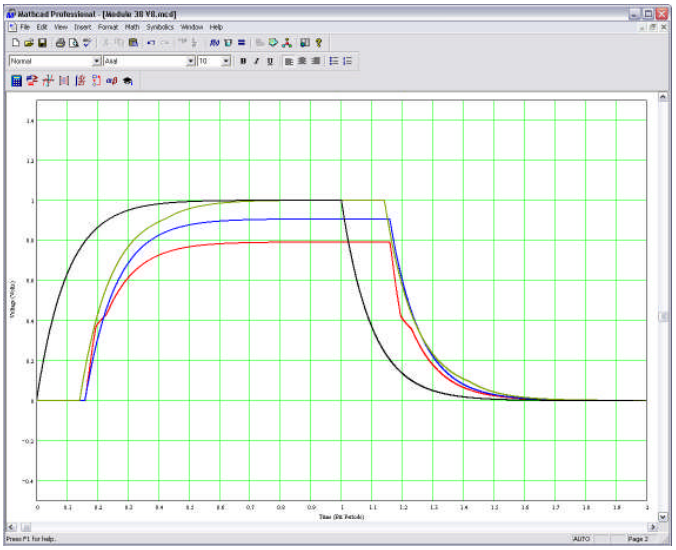

Fig. 2. Input (black) pulse, and output pulses when the 50Ω termination is close to the load (brown), before and away from the load (red), and after and away from the load (blue). The source impedance is 50Ω.

As can be seen from Figure 2, placing the termination before and away from the load produces significant signal degradations along the risetime and falltime, as well as a reduced peak value. On the other hand, placing the termination resistor after and away from the load does not exhibit such signal degradations along the rising and falling edges, and the peak voltage is larger. For comparative purposes, the brown curve corresponds to the optimal situation in which the termination resistor is close to the load,

and the black curve corresponds to the input transmitted pulse. Figure 3 shows the corresponding eye patterns.

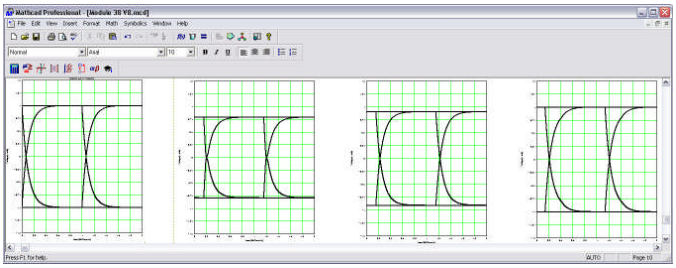

Fig. 3. From left to right, the eye patterns correspond to the input eye pattern, the eye pattern due to placing the resistor before and away from the load, the eye pattern due to placing the resistor after and away from the load, and the eye pattern when the resistor is close to the load.

At this point, it is instructive to determine the performance of the system when the source impedance is reduced from 50Ω to 6Ω. In this situation, Figures 4-5 highlight the input and output waveforms.

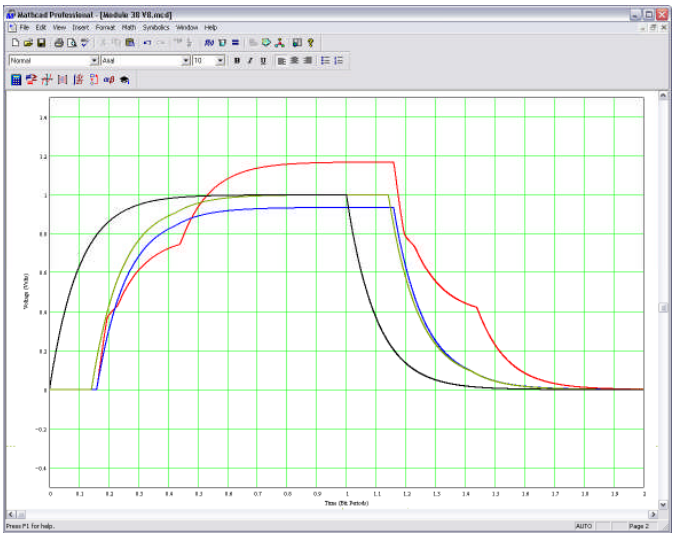

Fig. 4. Input (black) pulse, and output pulses when the 50Ω termination is close to the load (brown), before and away from the load (red), and after and away from the load (blue). The source impedance is 6Ω.

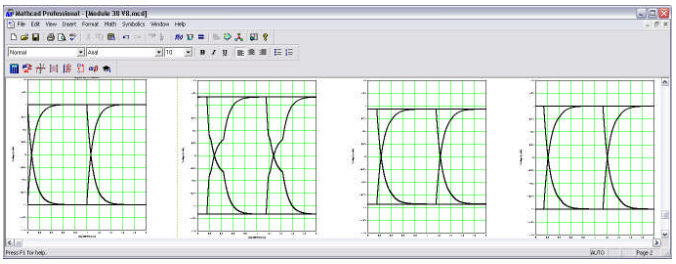

Fig. 5. From left to right, the eye patterns correspond to the input eye pattern, the eye pattern due to placing the resistor before and away from the load, the eye pattern due to placing the resistor after and away from the load, and the eye pattern when the resistor is close to the load.

Figures 4-5 clearly show that placing the load termination resistor after and away from the load produces the best signal integrity performance when the resistor can not be placed close to the load. Therefore, for sources that are either matched to the transmission line, or have low source impedances, the optimal location of the termination resistor is after and away from the high impedance load.

III. Conclusions

Based upon the previous research, it was disclosed that the termination resistor should be placed after and away from the load whenever this resistor can not be placed close to the load. This design guideline works well whenever the source impedance either matches the impedance of the transmission line, or when the source impedance is small. In either case, the maximum reduction in the noise margin was shown to be only 10%, and occurs when the source impedance exactly matches the impedance of the 50Ω transmission line. The material covered throughout this paper can be studied through the interactive signal integrity learning environment that is available at the following website: www.the-signal-and-power-integrity-institute.com .