Guidance For Scrambling Data Signals For EMC Compliance

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Abstract*—Scramblers can be used to help mitigate the radiated emissions from inherently periodic data signals. A previous paper [1] described such benefits when using a 7-bit scrambler to reduce the radiated emissions from the fourth harmonic of a data signal that contained a 21MHz fundamental frequency interval. This paper attempts to provide engineering guidance when determining how to use and implement a data scrambler that is based upon an n-bit maximum length feedback shift register. In particular, it is shown that the serial-in/serial-out manner in which the input data is scrambled produces a constraint on the maximum frequency in which the scrambler can operate. This frequency, denoted f_{max}, depends upon the semiconductor technologies that are used to implement the scrambler. In applications where the input bit rate of the scrambler is very close to f_{max}, the scrambler might exhibit performance degradations due to the input bit rate approaching this limit. In these situations, the scrambling operation can still be accomplished with the same scrambler; however, the scrambling can be performed on groups of input bits. This paper highlights the performances of 4-bit, 5-bit, 6-bit, and 7-bit scramblers when the data from a 100Mbs highly periodic signal is scrambled in groups of 2, 3, 4, or 5 bits at a time, enabling the scrambler to operate at frequencies of $f_{max}/2$, $f_{max}/3$, $f_{max}/4$, and $f_{max}/5$. It is shown that scrambling groups of input bits up to 3 bits at a time produces robust results. Therefore, for providing some performance margin, serial-in/serial-out scramblers that are limited to operating frequencies of f_{max} can be used to scramble data signals with input bit rates very close to f_{max} by scrambling groups of input bits up to 3 bits at a time.

I. Introduction

Sometimes a data signal can cause an EMC noncompliance performance issue due to its inherent periodicity in the time-domain. For example, if a baseband data pulse train includes an embedded periodic pattern, discrete line components will appear within the signal's power spectrum. In this case, some of the peaks of the power spectrum may exceed the permissible EMC levels. One means of mitigating the peak levels of the signal's harmonics is to scramble the data signal. The primary purpose of energy dispersal or scrambling techniques is to reduce the power levels of individual discrete spectral lines, subsequently improving the EMC performance of the system that contains such inherently periodic signals. This energy-dispersal feature can be accomplished by transforming the inherently periodic data signal into more of a random data signal. This kind of scrambling operation has been adopted in some industry standard signaling schemes [2].

It is generally well known that the power from a signal is inversely related to its inherent periodicity. The shorter the period, the more power the signal will radiate in its environment. One of the most periodic signals is a clock signal. In this case, the clock signal alternates between logic high and logic low levels very regularly. This short periodicity is one reason why clock signals usually generate significant radiation levels. Other data signals may also have embedded periodic components. One strategy that can be used to reduce the noise levels from a signal that is inherently periodic is to increase the inherent periodicity of the signal. This operation can be realized by scrambling this signal with a pseudorandom signal having a deterministic period that is significantly longer than the embedded periods of the data signal. Thus, scramblers cause periodic signals to appear more random. A scrambler can be implemented with an N-bit tapped shift register, and is capable of generating a scrambled output sequence in which the minimum period is 2^N - 1 bits [2],[3]. This extension of the period of the data signal is very similar in principle to the technique that is used to spread the spectrum in direct sequence spread spectrum systems [2],[3]. In this case, an RF modulated data signal is mixed with a code signal that has a very long deterministic period, and whose chip rate is much larger than the bit rate of the modulated signal. The mixing produces a signal whose spectrum is spread significantly more so than the original spectrum of the RF modulated data signal. In addition to spreading the spectrum of the RF modulated data signal, the maximum amplitude of the spectrum of the mixed signal is significantly lower than the maximum amplitude of the spectrum from the original RF modulated signal before mixing.

Scrambling performs a similar kind of a spectral spreading effect, however, to a baseband data signal, not an RF modulated signal. Many candidate code signals can be used to scramble the data signal. One such class of code signals is the class of maximum length sequences or m-sequences. In this case, these pseudorandom code signals can have periods up to $6.19(10^{26})$ bits [3]. Of course, for the purpose of spreading the spectrum of the data signal to acceptable levels, much shorter pseudorandom code signals should be used, such as 31-bit, 63-bit, or 127-bit periodic code signals.

II. Theoretical Foundation

Figure 1 shows a 7-bit scrambler that is implemented through the use of a tapped shift register feedback structure. The initial load of the register is 1011001. This kind of implementation is referred to in the industry as a Fibonacci scrambler [3]. In this case, the elements of the shift register are connected to modulo-2 adders in a feedback configuration. Whether a connection exists from each element of the shift register to a given modulo-2 adder depends upon the value of

the a_i coefficients. Suitable values of the a_i coefficients are shown in Figure 2, in which a binary value of *1* implies a connection, and a binary value of *0* implies no connection [3]. From Figure 2, the top set of coefficients would produce the simplest hardware implementation of the 7-bit scrambler and were used as the connection coefficients for all results presented in this paper.

The goal of the scrambler is to increase the inherent periodicity of the data signal, while reducing the peak levels of the signal's harmonics. A fundamental limitation of the scrambler structure shown in Figure 1 is the maximum operating frequency. In this case, the maximum operating frequency is given by the following equation [1]:

$$f_{\max} = \frac{1}{T_{P-FF} + T_{SU-FF} + T_{P-XOR} + 6T_{CK-SK}}$$

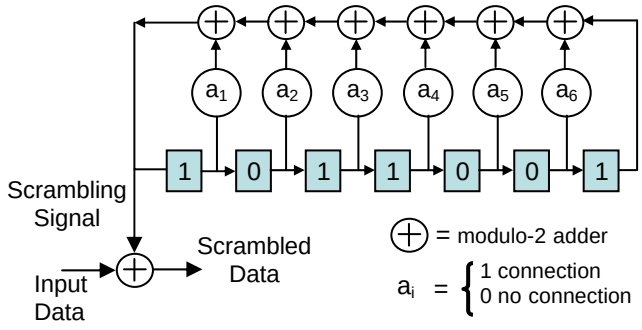

Fig.1. Implementation of a 7-bit scrambler.

$a_1 = a_2 = a_4 = a_5 = a_6 = 0, a_3 = 1$
$a_1 = a_2 = a_3 = 1, a_4 = a_5 = a_6 = 0$
$a_1 = a_5 = a_6 = 0, a_2 = a_3 = a_4 = 1$
$a_3 = 0, a_1 = a_2 = a_4 = a_5 = a_6 = 1$
$a_1 = a_2 = a_3 = a_4 = a_5 = 1, a_6 = 0$
$a_1 = a_3 = a_5 = 0, a_2 = a_4 = a_6 = 1$
$a_2 = a_3 = a_4 = a_5 = a_6 = 0, a_1 = 1$
$a_2 = a_4 = a_5 = 0, a_1 = a_3 = a_6 = 1$
$a_1 = a_3 = a_4 = 0, a_2 = a_5 = a_6 = 1$

Fig. 2. Possible values of the a_i coefficients.

The variable $T_{P\text{-}FF}$ represents the propagation delay from the triggering edge of a clock pulse to the output, Q, of a given D flip flop. The variable $T_{SU\text{-}FF}$ represents the setup time of a D flip flop, whereas the variable $T_{P\text{-}XOR}$ is the propagation delay of the XOR gate. The variable $T_{CK\text{-}SK}$ represents the clock skew between adjacent D flip flops. When $T_{P\text{-}FF}$ = 15ns, $T_{SU\text{-}FF}$ =10ns, $T_{P\text{-}XOR}$=3ns, and $T_{CK\text{-}SK}$ = 10ps, the maximum operating frequency is f_{max} = 35.6MHz. Therefore, the serial-in/serial-out scrambler is typically used for low to medium operating frequencies. Although the scrambling operation can be performed on a bit-by-bit basis on the input data, it is possible to scramble the data in groups of input bits. By doing so, the operating frequency of the serial-in/serial-out scrambler can be reduced to lower frequencies, while providing some operational margin.

For example, when the input data is scrambled in groups of two bits, three bits, four bits, or five bits at a time, the operating frequency of the scrambler can be reduced to $f_{max}/2$, $f_{max}/3$, $f_{max}/4$, and $f_{max}/5$, respectively. The impact of scrambling the input data in groups of bits on reducing the radiated emissions from the scrambled data is of interest. To help quantify this performance, a 50MHz clock signal is scrambled in groups of one bit, two bits, three bits, four bits, and five bits. It is also of interest to understand the impact of the size of the scrambler on reducing the radiated emissions from the input data when scrambling the input data in groups of bits. It is understood that scrambling a clock signal in this manner is typically not encountered in practice; however, it is instructive to see the impact of the scrambler on reducing the harmonic levels of a highly periodic signal, from a simulation perspective. Other more practical means exist for reducing the radiated emissions from clock signals [5], [6].

To help initiate this analysis, Figure 3 highlights the baseline simulation results when a 50MHz clock signal is scrambled with 4-bit, 5-bit, 6-bit, and 7-bit scramblers one bit at a time, and when f_{max} = 100MHz. Figure 4 highlights the resulting power spectra from this simulation. All simulations were based upon a model that was derived by the author.

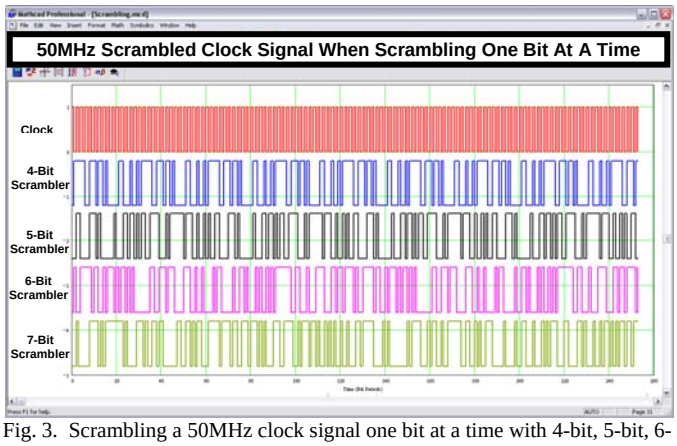

Fig. 3. Scrambling a 50MHz clock signal one bit at a time with 4-bit, 5-bit, 6-bit, and 7-bit scramblers, and when f_{max} = 100MHz.

The 4-bit scrambler produces a scrambled signal with a 30-bit period. The 5-bit scrambler produces a scrambled signal with a 62-bit period. Finally, the 6-bit and 7-bit scramblers produce scrambled signals with 126-bit and 254-bit periods,

respectively. As can be seen from Figure 4, the 7-bit scrambler produces the lowest peak envelope, and produced about 42dB of attenuation to the 50MHz fundamental harmonic frequency of the clock. One the other hand, the 4-bit scrambler produced about 24dB of attenuation to the 50MHz harmonic frequency of the clock.

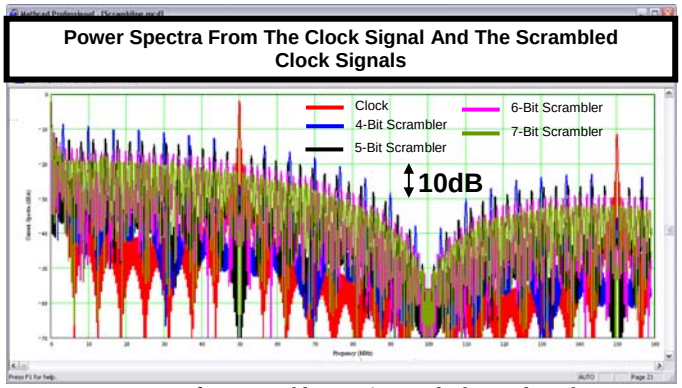

Fig. 4. Power spectra from scrambling a 50MHz clock signal one bit at a time with 4-bit, 5-bit, 6-bit, and 7-bit scramblers.

When scrambling the input data in groups of two bits at a time, Figure 5 shows the resulting scrambled signals from the simulation. Scrambling two bits at a time means that two consecutive input data bits are scrambled by the same scrambling bit. In this case, the 4-bit scrambler still produces a scrambled signal with a 30-bit period, while the 7-bit scrambler also still produces a scrambled signal with a 254-bit period. Figure 6 shows the resulting power spectra. In this situation, the 7-bit scrambler still produces about 42dB of attenuation to the 50MHz harmonic of the clock, whereas the 4-bit scrambler produces about 21.2dB of attenuation to this frequency. Figures 7-8 show the results from the simulation when the input bits are scrambled three bits at a time.

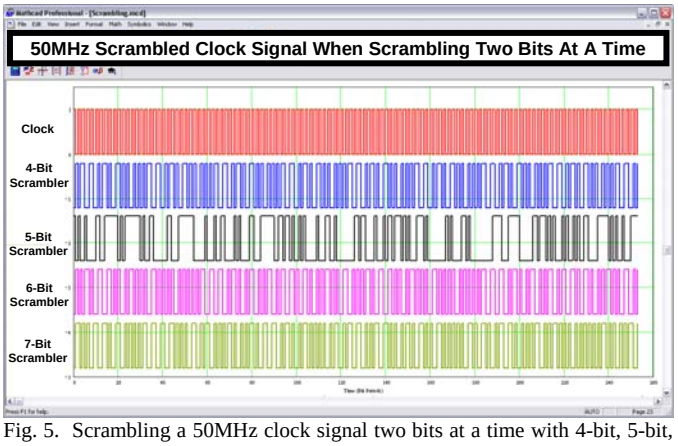

Fig. 5. Scrambling a 50MHz clock signal two bits at a time with 4-bit, 5-bit, 6-bit, and 7-bit scramblers, and when f_{max} = 100MHz.

Scrambling bits three at a time means that three consecutive input bits are scrambled by the same scrambling bit. In this situation, the 4-bit scrambler produced a scrambled signal with a period of 90 bits, which is a factor of three times the period when scrambling input bits either one at a time or two at a time. This result, although correct, is not intuitive. The attenuation values at 50MHz for the 4-bit and 7-bit scramblers are 22dB and 30dB, respectively. Note the significant differences between Figures 4, 6, and 8 at other frequencies.

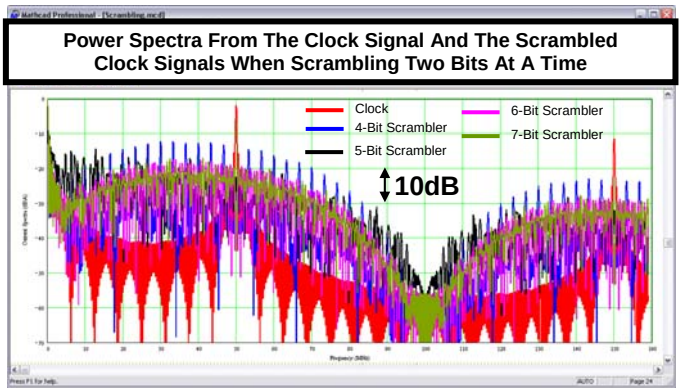

Fig. 6. Power spectra from scrambling a 50MHz clock signal two bits at a time with 4-bit, 5-bit, 6-bit, and 7-bit scramblers.

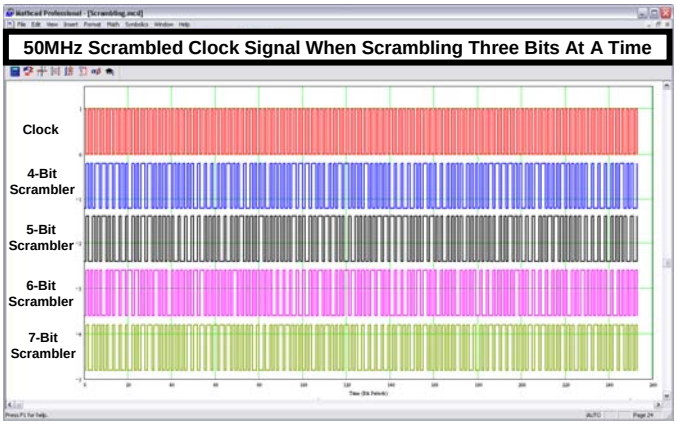

Fig. 7. Scrambling a 50MHz clock signal three bits at a time with 4-bit, 5-bit, 6-bit, and 7-bit scramblers, and when f_{max} = 100MHz.

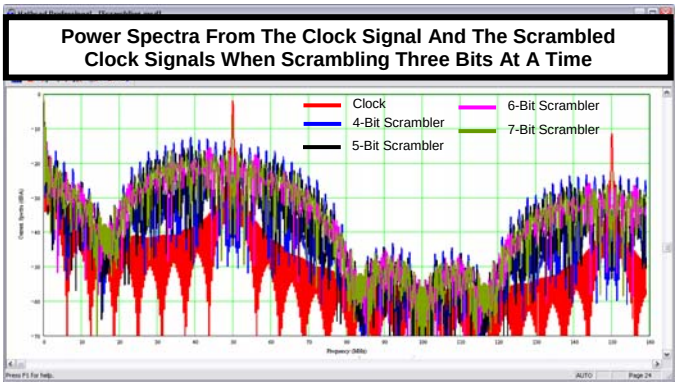

Fig. 8. Power spectra from scrambling a 50MHz clock signal three bits at a time with 4-bit, 5-bit, 6-bit, and 7-bit scramblers.

When the input data bits are scrambled four bits at a time, the scrambled data appears much less random than when scrambling the input bits one bit at a time, or two bits at a time. Scrambling the input bits four bits at a time means that four consecutive input bits are scrambled by the same scrambling bit. Figures 9 and 10 highlight the simulation results. The attenuation values at the 50MHz fundamental harmonic frequency for the 4-bit and 7-bit scramblers are 21.2dB and

32.5dB, respectively. Although the attenuation at 50MHz is robust, the power spectra around 50MHz is significantly higher than when scrambling the input data either one bit at a time or two bits at a time.

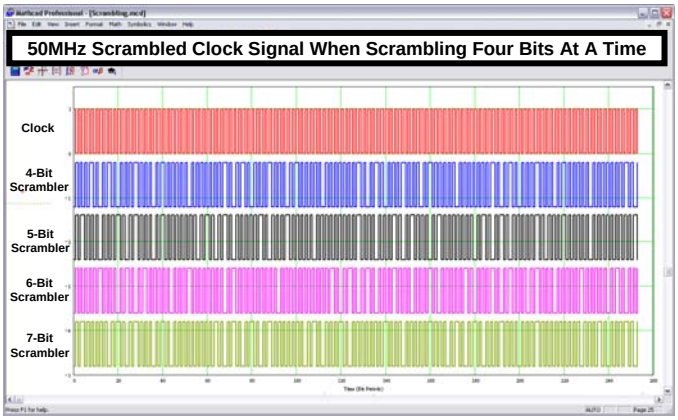

Fig. 9. Scrambling a 50MHz clock signal four bits at a time with 4-bit, 5-bit, 6-bit, and 7-bit scramblers, and when f_{max} = 100MHz.

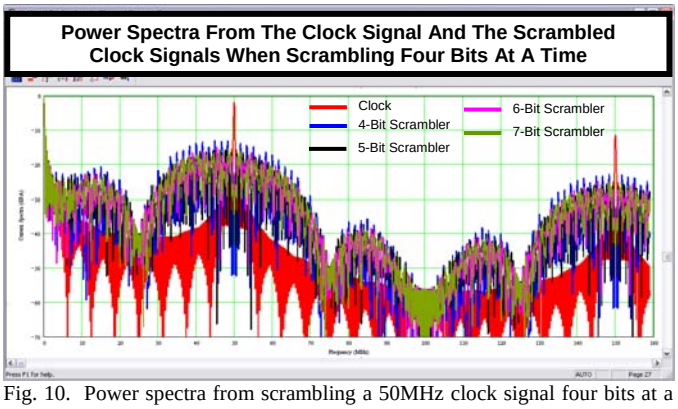

Fig. 10. Power spectra from scrambling a 50MHz clock signal four bits at a time with 4-bit, 5-bit, 6-bit, and 7-bit scramblers.

For the sake of completion, Figures 11 and 12 highlight the simulation results when the input data bits are scrambled five bits at a time. Scrambling input bits five bits at a time means that five consecutive input bits are scrambled with the same scrambling bit. The attenuation values at the 50MHz fundamental harmonic frequency for the 4-bit and 7-bit scramblers are 20.5dB and 25.1dB, respectively. As expected, the signal attenuation at 50MHz decreases as the size of the grouping of the input bits increases in value. As the grouping size of the input bits increases in value, the scrambled signal appears less random, and the scrambled signal starts to look more like the original clock signal from time-domain and frequency-domain perspectives. As the grouping of the input bits increases in value, the power spectra of the scrambled signals begin to converge to the power spectrum of the original 50MHz clock signal, which is undesirable. As such, the grouping size of the input bits should be restricted to no more than three bits. Restricting the grouping of input bits to two bits provides a reduction in the operating frequency of the scrambler from f_{max} to f_{max} /2, resulting in a 50% improved operating margin. This improvement may be all that is needed for the given application.

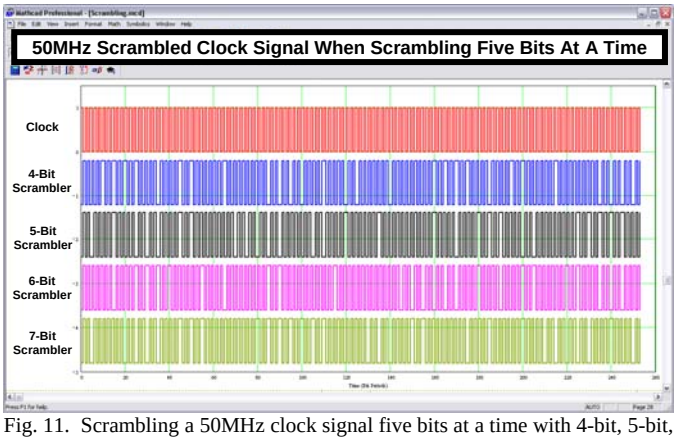

Fig. 11. Scrambling a 50MHz clock signal five bits at a time with 4-bit, 5-bit, 6-bit, and 7-bit scramblers, and when f_{max} = 100MHz.

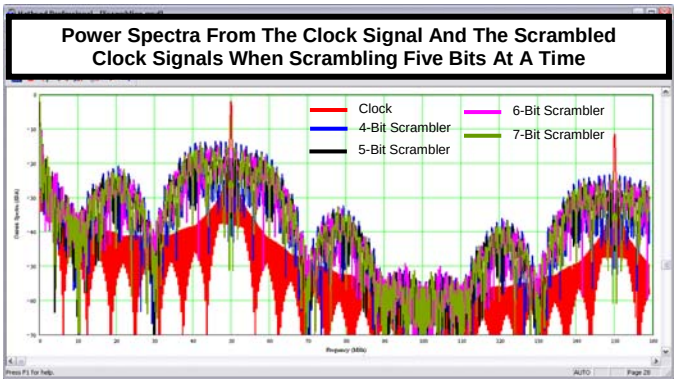

Fig. 12. Power spectra from scrambling a 50MHz clock signal five bits at a time with 4-bit, 5-bit, 6-bit, and 7-bit scramblers.

Additional insight into the performance of the serial-in/serial-out scrambler can be gleaned by determining the frequency responses of these scramblers in the 1-bit, 2-bit, 3-bit, 4-bit, and 5-bit input data grouping modes. For simplicity, only the frequency responses for the 4-bit and 7-bit scramblers are shown in this paper. Figure 13 shows the derived frequency responses for the case in which the input data is scrambled one bit at a time.

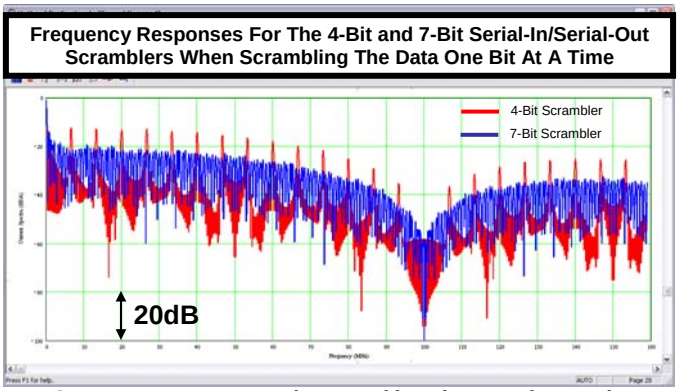

Fig. 13. Frequency responses when scrambling the input data one bit at a time.

When selecting a suitable scrambler and its operating mode, the frequency responses can be used to provide some guidance. For example, if a 50MHz harmonic frequency needs to be

scrambled, then the 7-bit scrambler in either the one-bit or two-bit operating modes can be used without significantly increasing the radiated emissions for frequencies around 50MHz. Figures 13-17 show that grouping input bits in groups of four or five bits should be avoided if scrambling an input data signal that contains an embedded 50MHz frequency component, for example. In this case, the choice of the scrambler should be based upon the attenuation provided to the 50MHz component, as well as the effect of the scrambler on frequencies outside of the 50MHz frequency.

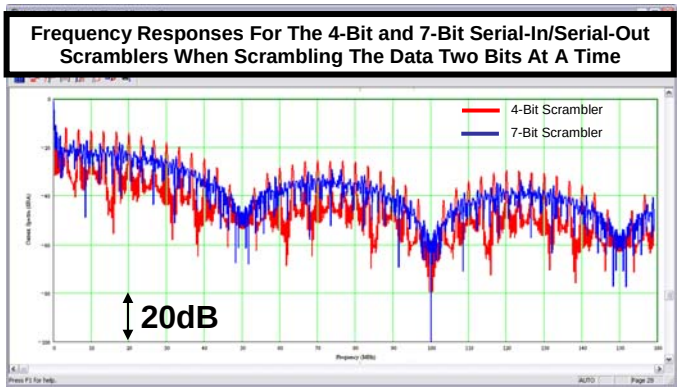

Fig. 14. Frequency responses when scrambling the input data two bits at a time.

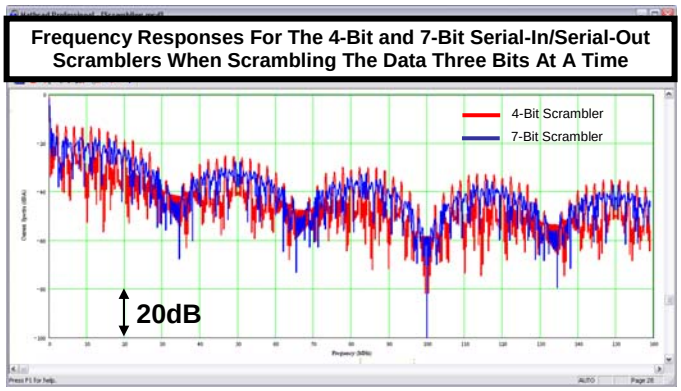

Fig. 15. Frequency responses when scrambling the input data three bits at a time.

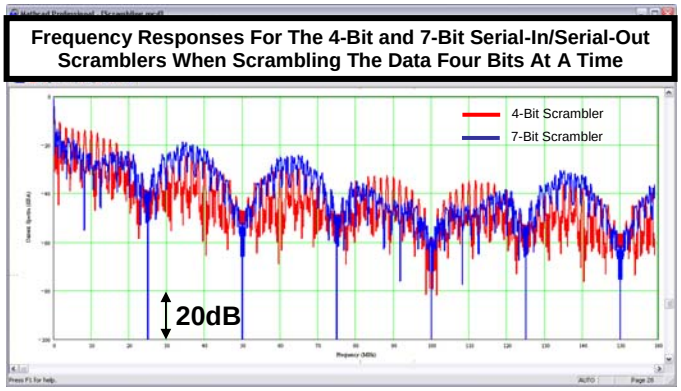

Fig. 16. Frequency responses when scrambling the input data four bits at a time.

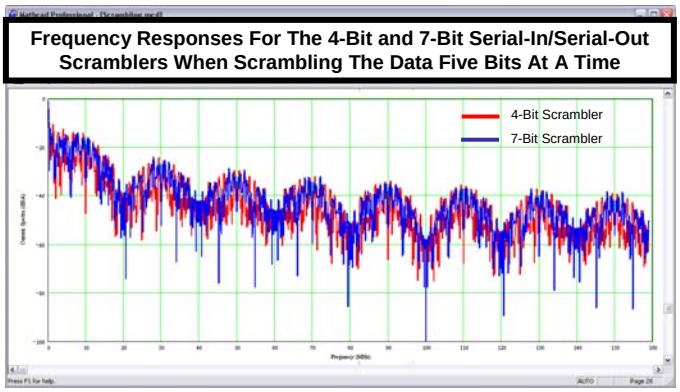

Fig. 17. Frequency responses when scrambling the input data five bits at a time.

III. Summary

This paper demonstrated the utility of scrambling data signals in order to reduce the radiated emissions from inherently periodic data signals. The fundamental structure of the serial-in/serial-out scrambler based upon the use of a shift register feedback structure was first described. Next, the fundamental frequency limitations of the scrambler were highlighted in order to provide an understanding of the technological limitations of such a scrambler. This limitation was captured in the form of a maximum scrambler operating frequency, f_{max}. It was next described how the scrambler could effectively scramble input data in groups of bits.

By doing so, the user does not attempt to operate the scrambler at an operating frequency of f_{max}. By scrambling the input data in groups of 2, 3, 4, or 5 bits at a time, it was demonstrated how effective scrambling in this manner can be accomplished by grouping input bits up to three bits at a time, as long as the size of the scrambler was at least 6 bits. Grouping input bits in groups of 4 or 5 bits at a time tended to cause excessive radiation at frequencies around the primary fundamental frequency of the input data. Therefore, effective mitigation of the radiation from inherently periodic data signals can be accomplished through the use of serial-in/serial-out scramblers, and when the input data bits are scrambled in groups of bits up to 2-3 bits. By doing so, plenty of operational margin is provided to the scrambler.

References

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